REMARKS

Claims 1-4 are pending in the application. Claims 1 and 2 have been amended by the present amendment. The amendments are fully supported by the specification as originally filed.

The specification was objected to because of certain typographical errors on page 1. It is respectfully asserted that Applicants made these corrections and other appropriate corrections in a Preliminary Amendment filed on November 21, 2003.

The title was objected to as not being descriptive. Applicants have adopted the Examiner's suggestion of a new title. It is believed that all objections to the specification have been overcome.

Applicants' claimed invention is directed to a method for fabricating a thermally-enhanced wafer-level chip scale package. As amended, claim 1 recites a step of attaching a thermally-conductive stiffener to the back side of a semiconductor wafer by means of a thermally-conductive adhesive layer, such as silver epoxy (see claim 2), where the thermally-conductive stiffener is free of electrical connection with the semiconductor wafer (see specification at page 5, lines 4-10 and 20-23; FIG. 4).

Referring to FIG. 1, the front side 10a of the semiconductor wafer 10 defines active surfaces of the chips, and the back side 10b of the semiconductor wafer defines **inactive** surfaces of the chips (see page 5, lines 4-10). As known to those of ordinary skill in the art, the inactive surface of a chip is not provided with terminals for external electrical connection, where such terminals are formed only on the active surface of the chip. Accordingly, the thermally-conductive stiffener 30 attached to the back side (inactive surface) of the semiconductor wafer 10 is not electrically connected to the semiconductor wafer (see FIG. 4).

As amended, claim 1 also recites a step of performing a singulation process to cut the thermally-conductive stiffener and cut apart each chip from the semiconductor wafer. This step is shown in FIG. 5 of the application, as described, e.g., on page 5, line 24 to page 6, line 2.

Claim 1 was rejected under 35 USC 102(b) as being anticipated by U.S. Patent 6,392,290 to Kasem et al. ("Kasem"). Claims 2 and 3 were rejected under 35 USC 103(a) as being unpatentable over Kasem in view of U.S. Patent 6,403,882 to Chen et al. ("Chen"). Claim 4 was rejected under 35 USC 103(a) as being unpatentable over Kasem in view of U.S. Patent 6,550,531 to Searls et al. These rejections are respectfully traversed.

Kasem does not teach or suggest a fabrication method including steps of: attaching a thermally-conductive stiffener to the back side of a semiconductor wafer by means of a thermally-conductive adhesive layer, where the thermally-conductive stiffener is free of electrical connection with the semiconductor wafer; and performing a singulation process to cut the thermally-conductive stiffener.

Referring to FIGS. 3A to 3C of Kasem, as cited in the Office Action, a package 10 includes a silicon chip 11 in which a power MOSFET is formed (see column 4, lines 39-42). The chip 11 has terminals on **both** sides of the chip, where source and gate terminals are located on the front side of the chip, and the drain terminal is located on the back side of the chip 11 (see column 4, lines 47-52).

As shown in FIGS. 3A to 3C, a support substrate 14 is attached to the back side of the chip 11 by an adhesive layer 13 (see column 4, lines 45-47). The drain terminal formed on the back side of the chip 11 is "electrically connected to the adhesive layer 13," such that the support substrate 14 is electrically connected to the drain terminal by means of the adhesive layer 13 (see column 4, lines 45-52).

In the Office Action, the support substrate 14 of Kasem was cited as corresponding to the Applicants' claimed "thermally-conductive stiffener." Even if the support substrate 14 is considered a stiffener, in Kasem, the support substrate 14 is electrically connected to the chip 11, whereas the Applicants' claimed invention requires the thermally-conductive stiffener to be free of electrical connection with the semiconductor wafer.

In the Applicants' claimed invention, only the front side (active surface) of the semiconductor wafer is provided for external electrical connection, whereas the thermally-conductive stiffener attached to the back side of the semiconductor wafer is **not** electrically connected to the semiconductor wafer.

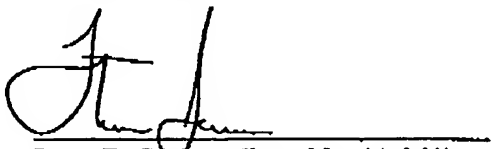
Moreover, there is no teaching or suggestion in Kasem of the step of "performing a singulation process to cut the thermally-conductive stiffener," as recited in claim 1.

Referring to claims 1 and 2, the thermally-conductive adhesive is attached to the semiconductor wafer by means of a thermally-conductive adhesive layer such as silver epoxy, such that the thermally-conductive stiffener serves as a heat-dissipating means for the chip to enhance overall heat-dissipation efficiency (see, e.g., specification at page 6, lines 12-14).

However, there is no teaching or suggestion in Kasem that the support substrate 14 is thermally conductive, or attached to the chip 11 by a thermally-conductive adhesive that serves as a heat-dissipation means. Therefore, even if Chen were somehow combined with Kasem, the proposed combination would not teach or suggest the thermally-conductive adhesive layer recited in claims 1 and 2.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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